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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,147	NGUYEN, HUNG T.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Witt et al., US Patent 5,651,125.

3. Referring to claim 1, Witt et al. have taught a mechanism for resource allocation in a processor, comprising:

   a. categorization logic, associated with an earlier pipeline stage, that generates instruction type information for instructions to be executed in said processor (column 13, lines 19-65, column 19, lines 21-40, In the decode stage the decoder decodes and generates an instruction opcode, or instruction type, and broadcasts to all of the functional units.);

   b. queueing logic, in which said instructions and said instruction type information are stored in an order based on a priority of said instructions (column 49, lines 6-14, column 13, lines 19-65, column 14, lines 6-15, Stored in a FIFO, where priority is determined by age.); and

   c. priority logic, associated with a later pipeline stage, that allocates functional units of said processor to execution of said instructions in said order based on said instruction type information (column 13, lines 19-65, column 14, lines 6-

15, The reservation stations are the priority logic that allocates functional units based on the opcode, or instruction type.).

4. Referring to claim 2, Witt et al. have taught the mechanism as recited in claim 1, as described above, and wherein said categorization logic causes said instruction type information to be stored and tagged in a queue containing said instructions (column 15, lines 56-61, column 23, lines 40-52, column 24, lines 36-52, Once the categorization logic, or decoder, broadcasts the opcodes to the functional units, it causes the opcode to be stored and tagged in a reservation station queue for a functional unit.).
5. Referring to claim 3, Witt et al. have taught the mechanism as recited in Claim l, as described above, and wherein said earlier pipeline stage is a fetch/decode stage of said processor (column 13, lines 19-65, column 19, lines 21-40).
6. Referring to claim 4, Witt et al. have taught the mechanism as recited in Claim 1, as described above, wherein said instructions are ungrouped when said categorization logic generates said instruction type information (column 19, lines 21-40, column 13, lines 57-65).
7. Referring to claim 5, Witt et al. have taught the method as recited in Claim 1, as described above, and wherein said instruction type information defines at least four categories of instruction (Figure 1A, Branch, ALU, Shifter, Load, Store).
8. Referring to claim 6, Witt et al. have taught the mechanism as recited in Claim 1, as described above, and wherein said priority logic employs separate allocation schemes depending upon categories defined by said instruction type information (The instruction type information defines the allocation scheme to be employed, i.e. a shift type opcode is

allocated to the shifter functional unit and a branch type opcode is allocated to the branch functional unit.).

9. Referring to claim 7, Witt et al. have taught the mechanism as recited in Claim 1, as described above, and wherein said processor is a digital signal processor (abstract).

10. Referring to claim 15, Witt et al. have taught a digital signal processor (DSP), comprising:

    a. a pipeline having stages (column 5, lines 40-48, stages are inherent);

    b. functional units coupled to said pipeline (Figure 1, elements 90, 95, 105,60, and 65);

    c. an instruction issue unit; coupled to said functional units, that wide-issues instructions for execution in said functional units (column 15, lines 41-56, Superscalar);

    d. categorization logic, associated with an earlier stage of said pipeline, that generates instruction type information for said instructions (column 13, lines 19-65, column 19, lines 21-40, In the decode stage the decoder decodes and generates an instruction opcode, or instruction type, and broadcasts to all of the functional units.);

    e. queueing logic, in which said instructions and said instruction type information are stored in an order based on a priority of said instructions (column 49, lines 6-14, column 13, lines 19-65, column 14, lines 6-15, Stored in a FIFO, where priority is determined by age.);and

f. priority logic, associated with a later stage of said pipeline, that allocates said functional units to said execution of said instructions based on said instruction type information (column 13, lines 19-65, column 14, lines 6-15, The reservation stations are the priority logic that allocates functional units based on the opcode, or instruction type.).

11. Claim 8 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

12. Claims 9 and 16 do not recite limitations above the claimed invention set forth in claim 2 and is therefore rejected for the same reasons set forth in the rejection of claim 2 above.

13. Claims 10 and 17 do not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

14. Claims 11 and 18 do not recite limitations above the claimed invention set forth in claim 4 and is therefore rejected for the same reasons set forth in the rejection of claim 4 above.

15. Claims 12 and 19 do not recite limitations above the claimed invention set forth in claim 5 and is therefore rejected for the same reasons set forth in the rejection of claim 5 above.

16. Claims 13 and 20 do not recite limitations above the claimed invention set forth in claim 6 and is therefore rejected for the same reasons set forth in the rejection of claim 6 above.

17. Claims 14 does not recite limitations above the claimed invention set forth in claim 7 and is therefore rejected for the same reasons set forth in the rejection of claim 7 above.

Response to Arguments

18. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100